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09/820,594	03/29/2001	Joseph Meehan	US010099	6145

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,594	MEEHAN ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-20* is/are allowed.

6)☒ Claim(s) *1-4,10-12 and 21* is/are rejected.

7)☒ Claim(s) *5-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 8/22/2005, have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicants' arguments but firmly believes that the cited reference to reasonably and properly meet the claimed limitations.

Claims 1, 10-12, and 21

(1) *Applicants' argument* – "Liberti discloses a FFT method and system for ratio combining; Liberti does not disclose a digital combiner circuit for receiving signals from said first receiver chips, said digital combiner circuit comprising (N -1) first buffer memories, (N -1) second buffer memories, and a clock synchronizing circuit as required in each of applicants' independent claims."

Examiner's response -- In response to applicant's argument as described as above paragraph, Liberti does disclose a digital combiner circuit (Fig.2 element 222 and part of element 218) for receiving signals from said first receiver chips (Fig.2 element 218), said digital combiner circuit comprising (N -1) first buffer memories (Fig.3 element 318 that located inside of Fig.2 element 218, here the examiner considers N = 2), (N -1) second buffer memories (Fig.4 element 406 that located inside of Fig.2 element 222, here the examiner considers N = 2), and a clock synchronizing circuit (Fig.2 element 216 and column 6 lines 48-54). For more explanation, the examiner considers the COMBINER DSP 222, TIMING

GENERATOR 216, and MEMORY 318 as a digital combiner as required in the instant application's each independent claim.

The TIMING GENERATOR 216 is coupled to the branch DSPs 218 and to the combiner DSP 222 to provide synchronization and timing for processing the plurality of digitized samples comprising the plurality of acknowledgment signals (Fig.2 element 216 and column 6 lines 48-54). The TIMING GENERATOR 216 functions as a clock synchronizing circuit as required in the instant application's each independent claim.

The MEMORY 318 located inside of the BRANDCH DSP 218 is used for temporary storage of interim values and calculations. It functions as a buffer memory. Since N is an integer number equal or greater than two, if N =2, there is only one buffer memory 318 required to meet the claim limitation as recited in the independent claims 1 and 21.

The MEMORY 406 located inside the COMBINER DSP 222 is used for temporary storage of interim values and calculations. It functions as a buffer memory. Since N is an integer number equal or greater than two, if N =2, there is only one buffer memory 406 required to meet the claim limitation as recited in the independent claims 1 and 21.

Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 103(a) with Libertis' reference is adequate.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liberti et al. (US 5,550,872) in view of the admitted prior art of the instant application and Wu (US 6,567,467).

- With regard claim1, Liberti et al. discloses an apparatus for improving reception in a receiver having N antennae (Fig.2 element 108), where N is an integer number with a value equal to or greater than 2 (Fig.2 element 108), comprising:

  N first receiver chips (Fig.2 element 218) each associated with one of said antennae (Fig.2 element 108);

  a digital combiner circuit (Fig.2 elements 218 and 222) for receiving signals from said first receiver chip (Fig.2 element 218), said digital combiner circuit comprising N -1 first buffer memories (Fig.2 element 218 and Fig.3 element 318), (N-I) second buffer memories (Fig.2 element 222 and Fig.3 element 406, *here, examiner is considering N = 2*) and a clock synchronizing module (Fig.2 element 216 and column 6 lines 48-54), with each buffer memory generating an output

signal (Fig.2 element 222 output, column 10 lines 63-67, *here, examiner is considering N =2*);

a common bus coupled to said first receiver chips and said digital combiner circuit (Fig.2 element 218 output to element 222 input, *here, examiner is considering N = 2*);

said clock synchronizing module capable of generating a delay signal (column 7 lines 38-59, where the elements 318 and 406 store and then calculated the received signal that is inherently generating a delayed signal.) and aligning said output signal of each buffer memory base on a common clock (column 5 lines 28-49 and column 6 lines 48-54);

said digital combiner circuit capable of generating a combined output signal Fig.2 element 222 output, column 10 lines 63-67, *here, examiner is considering N =2*; and

a computer (inside of Fig.1 element 120 computer modem) for receiving said combined output signal of said digital combiner circuit (Fig.2 element 222 output).

Liberti et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching -

a) each chip comprising a front-end section, equalizer, and a back-end section

b) the computer including said second receiver chip comprising a front-end section, equalizer and a back-end section.

With regard a), the admitted prior art of the instant application teaches a receiver with a single chip including a Front-End and Equalizer and Back-End (Fig.1

elements 15-18) in order to reduce the receiver cost. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the apparatus as taught by the admitted prior art of the instant application in which, have a single chip comprising a front-end section, equalizer and a back-end section, into Libertis' Branch DSP (fig.2 element 218) so as to reduce the receiver cost.

Liberti et al. and the admitted prior art of the instant application disclose all of the subject matter as described in the above paragraph except for specifically teaching -

b) the computer including said second receiver comprising a front-end section, equalizer and a back-end section.

However, Wu teaches a network interface controller (NIC) inside a computer system (Abstract lines 10-13, column 1 lines 63-67, and column 3 lines 5-20) with an equalizer (Fig.1 element 104). It is inherent that there must be a front- end section to interface the received input signal and it is also inherent that there must be a back-end circuit to interface or receive the equalizer output signal in order to re duce the cost of receiver ASIC and NIC (column 1 lines 45-60).

Liberti et al. and the admitted prior art of the instant application and Wu teaches a second receiver with discrete circuit, front-end, equalizer, and back-end circuit, in a NIC except for specifically teaching the second receiver is a integrated chip. It would have been obvious to one having ordinary skill in the art at the time the invention was made to integrated discrete circuit, front-end, equalizer, and back-

end circuit into a chip, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. Howard v. Detroit Stove works, 150 U.S. 164 (1893).

- With regard claim 2, Liberti et al. further discloses N tuners (Fig.2 element 214) for receiving IF signals from each antenna and converting said IF signals to low IF signals before forwarding said low IF signals (Fig.2 element 220 input) to said first receiver chips. It is inherent that the receiver (214) convert the RF signal to said low IF signal and feed to analog to digital converter input (Fig.2 element 220).
- With regard claim 3, Liberti et al. further discloses N analog to digital converters (Fig.2 element 220).
- With regard claim 4, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liberti et al. (US 5,550;872) and the admitted prior art of the instant application and Wu (US 6,567,467) as applied to claim 1 above, and further in view of Miller (US 6,438,570).

- With regard claim 10, Liberti et al. and the admitted prior art of the instant application and Wu disclose a combiner with DSP as described in the above paragraph except for specifically teaching digital combiner is an FPGA. However, Miller teaches a FPGA that has been used to implement digital signal processing (DSP) algorithms which are inherently parallel and normally require multiple DSP microprocessors (column 1 lines 35-45) in order to meet the high

data rates and improve the performance and reduce the cost (column 1 lines 46-50). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement the FPGA as taught by Miller to replace the DSP combiner of the Liberti et al. and the admitted prior art of the instant application and Wus' so as to improve the performance and reduce the cost.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liberti et al. (US 5,550,872) and the admitted prior art of the instant application and Wu (US 6,567,467) as applied to claim 1 above, and further in view of Moss (US 4,151,609).

- With regard claim 10, Liberti et al. and the admitted prior art of the instant application and Wu disclose all subject matter as described in the above paragraph except for specifically teaching each of (N-1) first buffer memories is a FIFO.

  However, Moss teaches a FIFO (Fig.1A and 1B) with the advantage of a FIFO memory system over a conventional sequential memory system that data can be entered into the memory system at various speeds while at the same time data can be taken out of the memory system at the same or different speeds (column 1 lines 34-50). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement the FIFO as taught by Miller to replace the memory of the Liberti et al. and the admitted prior art of the instant application and Wus' so as to improve the performance and reduce the cost.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liberti et al. (US 5,550,872) and the admitted prior art of the instant application and Wu (US 6,567,467) as applied to claim 1 above, and further in view of Kao et al. (US 4,720,812).

- With regard claim 10, Liberti et al. and the admitted prior art of the instant application and Wu disclose all subject matter as described in the above paragraph except for specifically teaching each of (N-1) second buffer memories is a RAM.

  However, Kao et al. teaches a RAM (column 1 lines 29-43) with the advantage of high density (i.e., high storage capability per unit volume), high speed and low cost (column 1 lines 34-36). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement the RAM as taught by Miller to replace the memory of the Liberti et al. and the admitted prior art of the instant application and Wus' so as to improve the speed and reduce the cost.

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liberti et al. (US 5,550,872) in view of Dixon et al. (US 5,568,443).

- With regard claim 21, Liberti et al. discloses a method for improving reception in a receiver having N antennae (Fig.2 element 108), where N (Fig.2 element 108) is an integer number that is greater than or equal to 2, comprising the steps of: receiving N signals from each respective N antennae (Fig.2 element 108) in receiver chips (Fig.2 element 218 and column 6 lines 1-54);

processing the signals in a digital combiner circuit (Fig.2 elements 218 and 222) that includes buffer memories (Fig.2 element s 212 and 218 and column 7 lines 38-59) and a clock synchronizing module (Fig.2 element 216 and column 6 lines 48-54), in order to generate a delay signal (column 7 lines 38-59, where the elements 318 and 406 store and then calculated the received signal that is inherently generating a delayed signal.) that synchronizes and combines output signals from the buffer memories to generate a combined output signal (Fig.2 element 222 output, column 10 lines 63-67); and

feeding the combined output signal to a single second receiver chip (Fig.2 element 206 and column 5 lines 28-39). Note that the element 206 is inherent as a receiver chip, since it is a microprocessor, MC6809, as cited, that receives the signal from the combiner chip 222 output.

Liberti et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching N plurality memories.

However, Dixon et al. teaches a single memory that includes N buffer memories (Fig.3, and Fig.4 element 61, column 1 line 50 – column 2 line 20, column 4 line 62 – column 5 line 6, and column 6 lines 36-45).

It is desirable to have a single memory comprising RAM and FIFO buffer memory in order to reduce the higher system cost and power consumption (column 1 lines 36-39). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the method as taught by Dixon et al. in which, have a single memory comprising RAM and FIFO buffer

memory, into Libertis' combiner chip so as to reduce the higher system cost and power consumption.

Allowable Subject Matter

8. Claims 13-20 are allowed.

9. Claims 5-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is an examiner's statement of reasons for allowance.

- The prior art fails to teach apparatus/method and methods of Claim 13 and 19 that specifically comprises the following:

-- The instant application is deemed to be directed to a non-obvious improvement over the invention patented in Pat. No. US 4,151,609, US 4,720,812, US 5,530,725, US 5,550,872, US 5,568,443, US 6,438,570. The improvement comprises that

With regard claim 13, "a third receiver chip for receiving from said digital combiner circuit, said third receiver chip comprising a front-end section, equalizer and a back-end section, wherein said third receiver chip receives said combined output signal at said back-end section; and a common bus coupled to said first and second tuners, to said first and second receiver chips and to said digital combiner circuit" as recited;

With regard claim 19, "weighting said first and second digital signals based on a signal quality indicator value; adding said weighted digital signals; passing a combined output signal into a back-end section of a third receiver chip." as recited.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

12. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

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